AMENDMENTS

IN THE CLAIMS:

Please cancel claims 1, 15-22, 34-38 and 40, and amend claims 2-3, 12, 23-27 and 39 as follows below:

1. (Canceled).

2. (Currently amended) ~~The method of claim 1,~~ A method for accessing ferroelectric memory cells in a ferroelectric memory device, the method comprising:

performing a read, restore, or write operation to access one or more ferroelectric memory cells along a selected wordline in a ferroelectric memory array; and

activating a non-selected wordline while a bitline and a plateline associated with the ferroelectric memory cells along the non-selected wordline are both substantially at a first voltage, and

further comprising at least one of the following:

wherein the first voltage is ground; or

activating one or more wordlines on power-up while corresponding bitlines and platelines are substantially at the first voltage; or

activating one or more wordlines before power-down while corresponding bitlines and platelines are substantially at the first voltage.

3. (Currently amended) ~~The method of claim 1, further comprising~~ A method for accessing ferroelectric memory cells in a ferroelectric memory device, the method comprising:

performing a read, restore, or write operation to access one or more ferroelectric memory cells along a selected wordline in a ferroelectric memory array; and

activating a non-selected wordline while a bitline and a plateline associated with the ferroelectric memory cells along the non-selected wordline are both substantially at a first voltage; and

activating other wordlines in a first plate group that includes cells along the selected wordline while bitlines and platelines associated with the first plate group are substantially at the first voltage to discharge storage nodes of cells of the first plate group.

4. (Original) The method of claim 3, wherein the wordlines in the first plate group are activated while the bitlines and platelines associated with the first plate group are substantially at the first voltage each time memory cells in the first plate group are accessed.

5. (Original) The method of claim 3, wherein the wordlines in the first plate group are activated while the bitlines and platelines associated with the first plate group are substantially at the first voltage every Nth time memory cells in the first plate group are accessed, N being an integer greater than 1.

6. (Original) The method of claim 3, wherein a first subset of wordlines in the first plate group are selectively activated while the bitlines and platelines associated with the first plate group are substantially at the first voltage each time memory cells in the first plate group are accessed, wherein the first subset of wordlines in the first plate group is chosen for selective activation according to a plate group access counter associated with the first plate group.

7. (Original) The method of claim 6, wherein the first subset is half of the wordlines in the first plate group and a second subset is the remaining half of the wordlines in the first plate group, wherein one of the first and second subsets of the wordlines in the first plate group are selectively activated while the bitlines and

platelines associated with the first plate group are substantially at the first voltage every time memory cells in the first plate group are accessed, wherein the subset to be activated is alternated every other time memory cells in the first plate group are accessed.

8. (Original) The method of claim 3, further comprising activating wordlines in a second plate group that does not include the selected wordline while bitlines and platelines associated with the second plate group are substantially at the first voltage.

9. (Original) The method of claim 8, wherein the second plate group is one of a plurality of non-selected plate groups that do not include the selected wordline, and wherein the second plate group is chosen for selective activation according to a non-accessed plate group counter or shift register.

10. (Original) The method of claim 8, wherein the first voltage is ground.

11. (Original) The method of claim 3, wherein the first voltage is ground.

12. (Currently amended) ~~The method of claim 1, further comprising~~ A method for accessing ferroelectric memory cells in a ferroelectric memory device, the method comprising:

performing a read, restore, or write operation to access one or more ferroelectric memory cells along a selected wordline in a ferroelectric memory array; and

activating a non-selected wordline while a bitline and a plateline associated with the ferroelectric memory cells along the non-selected wordline are both substantially at a first voltage; and

activating wordlines in a plate group that does not include the selected wordline while bitlines and platelines associated with the ~~second~~ plate group are substantially at the first voltage.

13. (Original) The method of claim 12, wherein the plate group is one of a plurality of non-selected plate groups that do not include the selected wordline, and wherein the plate group is chosen for selective activation according to a non-accessed plate group counter or shift register.

14. (Original) The method of claim 12, wherein the first voltage is ground.

15-22. (Canceled).

23. (Currently amended) ~~The device of claim 22,~~ A ferroelectric memory device, comprising:

an array of ferroelectric memory cells arranged in rows and columns, the cells individually comprising at least one ferroelectric cell capacitor having a first terminal and a second terminal coupled with a plateline, and at least one cell transistor adapted to selectively couple the first cell capacitor terminal to an array bitline associated with an array column according to an array wordline, wherein rows of the memory cells are coupled with a corresponding wordline and a plateline, wherein the array comprises a plurality of plate groups, and wherein cells along a plurality of wordlines in a plate group are coupled with a common plateline;

a control system coupled with the array, the control system providing wordline and plateline signals to the array during read, restore, and write operations to access one or more ferroelectric memory cells along a selected wordline in the array; and

a wordline pulse system coupled with the control system and with the array, the wordline pulse system being adapted to activate one or more non-selected wordlines in the array while one or more bitlines and platelines associated with ferroelectric memory cells along the one or more non-selected wordlines are both substantially at a first voltage; and

further comprising at least one of the following:

wherein the first voltage is ground; or

wherein the wordline pulse system comprises a plurality of plate group access counters, the plate group access counters being individually associated with plate groups of the array and indicating a number of accesses of cells in the associated plate group, wherein the wordline pulse system selectively activates a first subset of wordlines in a first plate group that includes cells along the selected wordline while the bitlines and platelines associated with the first plate group are substantially at the first voltage each time memory cells in the first plate group are accessed, and wherein the first subset of the wordlines in the first plate group is chosen for selective activation according to a plate group access counter associated with the first plate group; or

wherein the wordline pulse system comprises a logic circuit and a plurality of wordline pulse drivers individually associated with wordlines in the array, the wordline pulse drivers individually comprising two NMOS transistors coupled in series between the logic circuit and the corresponding wordline for selectively activating the corresponding wordline; or

wherein the wordline pulse system comprises a logic circuit and a plurality of wordline pulse drivers individually associated with wordlines in the array, the wordline pulse drivers individually comprising an NMOS transistor coupled in series between the logic circuit and the corresponding wordline for selectively activating the corresponding wordline.

24. (Currently amended) The device of claim ~~22~~ 23, wherein the wordline pulse system is adapted to activate non-selected wordlines in a first plate group that includes cells along the selected wordline before, during, or after the read, restore, or write operation while bitlines and platelines associated with the ferroelectric memory cells along wordlines in the first plate group are substantially at a first voltage.

25. (Currently amended) The device of claim ~~22~~ 23, wherein the wordline pulse system is adapted to activate wordlines in a second plate group that does not include cells along the selected wordline before, during, or after the read, restore, or write operation while bitlines and platelines associated with the ferroelectric memory cells along wordlines in the second plate group are substantially at the first voltage.

26. (Currently amended) The device of claim ~~22~~ 23, wherein the wordline pulse system is further adapted to activate the selected wordline while a bitline and a plateline associated with memory cells along the selected wordline are substantially at the first voltage.

27. (Currently amended) ~~The device of claim 22,~~ A ferroelectric memory device, comprising:

an array of ferroelectric memory cells arranged in rows and columns, the cells individually comprising at least one ferroelectric cell capacitor having a first terminal and a second terminal coupled with a plateline, and at least one cell transistor adapted to selectively couple the first cell capacitor terminal to an array bitline associated with an array column according to an array wordline, wherein rows of the memory cells are coupled with a corresponding wordline and a plateline, wherein the array comprises a plurality of plate groups, and wherein cells along a plurality of wordlines in a plate group are coupled with a common plateline;

a control system coupled with the array, the control system providing wordline and plateline signals to the array during read, restore, and write operations to access one or more ferroelectric memory cells along a selected wordline in the array; and

a wordline pulse system coupled with the control system and with the array, the wordline pulse system being adapted to activate one or more non-selected wordlines in the array while one or more bitlines and platelines associated with ferroelectric memory

cells along the one or more non-selected wordlines are both substantially at a first voltage, and

wherein the wordline pulse system is further adapted to activate wordlines in a first plate group that includes cells along the selected wordline while bitlines and platelines associated with the ferroelectric memory cells along wordlines in the first plate group are substantially at the first voltage.

28. (Original) The device of claim 27, wherein the wordline pulse system activates wordlines in the first plate group while the bitlines and platelines associated with the first plate group are substantially at the first voltage each time memory cells in the first plate group are accessed.

29. (Original) The device of claim 27, wherein the wordline pulse system activates wordlines in the first plate group while the bitlines and platelines associated with the first plate group are substantially at the first voltage every Nth time memory cells in the first plate group are accessed, N being an integer greater than 1.

30. (Original) The device of claim 27, wherein the wordline pulse system comprises a plurality of plate group access counters, the plate group access counters being individually associated with plate groups of the array and indicating a number of accesses of cells in the associated plate group, wherein the wordline pulse system selectively activates a first subset of wordlines in the first plate group while the bitlines and platelines associated with the first plate group are substantially at the first voltage each time memory cells in the first plate group are accessed, and wherein the first subset of the wordlines in the first plate group is chosen for selective activation according to a plate group access counter associated with the first plate group.

31. (Original) The device of claim 30, wherein the first subset is half of the wordlines in the first plate group and a second subset is the remaining half of the

wordlines in the first plate group, wherein the wordline pulse system selectively activates one of the first and second subsets of the wordlines in the first plate group while the bitlines and platelines associated with the first plate group are substantially at the first voltage every time memory cells in the first plate group are accessed, and wherein the subset to be activated is alternated every other time memory cells in the first plate group are accessed.

32. (Original) The device of claim 27, wherein the wordline pulse system is further adapted to activate wordlines in a second plate group that does not include cells along the selected wordline while bitlines and platelines associated with the ferroelectric memory cells along wordlines in the second plate group are substantially at the first voltage.

33. (Original) The device of claim 32, wherein the wordline pulse system comprises a non-accessed plate group counter or shift register indicating a particular plate group of the array, wherein the second plate group is one of a plurality of non-selected plate groups that do not include the selected wordline, and wherein the second plate group is chosen for selective activation according to the non-accessed plate group counter or shift register.

34-38. (Canceled).

39. (Currently amended) ~~The device of claim 37,~~ A ferroelectric memory device, comprising:

an array of ferroelectric memory cells arranged in rows and columns;

a control system coupled with the array, the control system providing wordline and plateline signals to the array during read, restore, and write operations to access one or more ferroelectric memory cells along a selected wordline in the array; and

a wordline pulse system to provide a pulse to one or more non-selected wordlines in the array while one or more bitlines and platelines associated with ferroelectric memory cells along the one or more non-selected wordlines are both substantially at a first voltage; and

further comprising at least one of the following:

wherein the first voltage is ground; or

wherein the wordline pulse system comprises a logic circuit and a plurality of wordline pulse drivers individually associated with wordlines in the array, the wordline pulse drivers individually comprising an NMOS transistor coupled in series between the logic circuit and the corresponding wordline for selectively activating the corresponding wordline.

40. (Canceled).